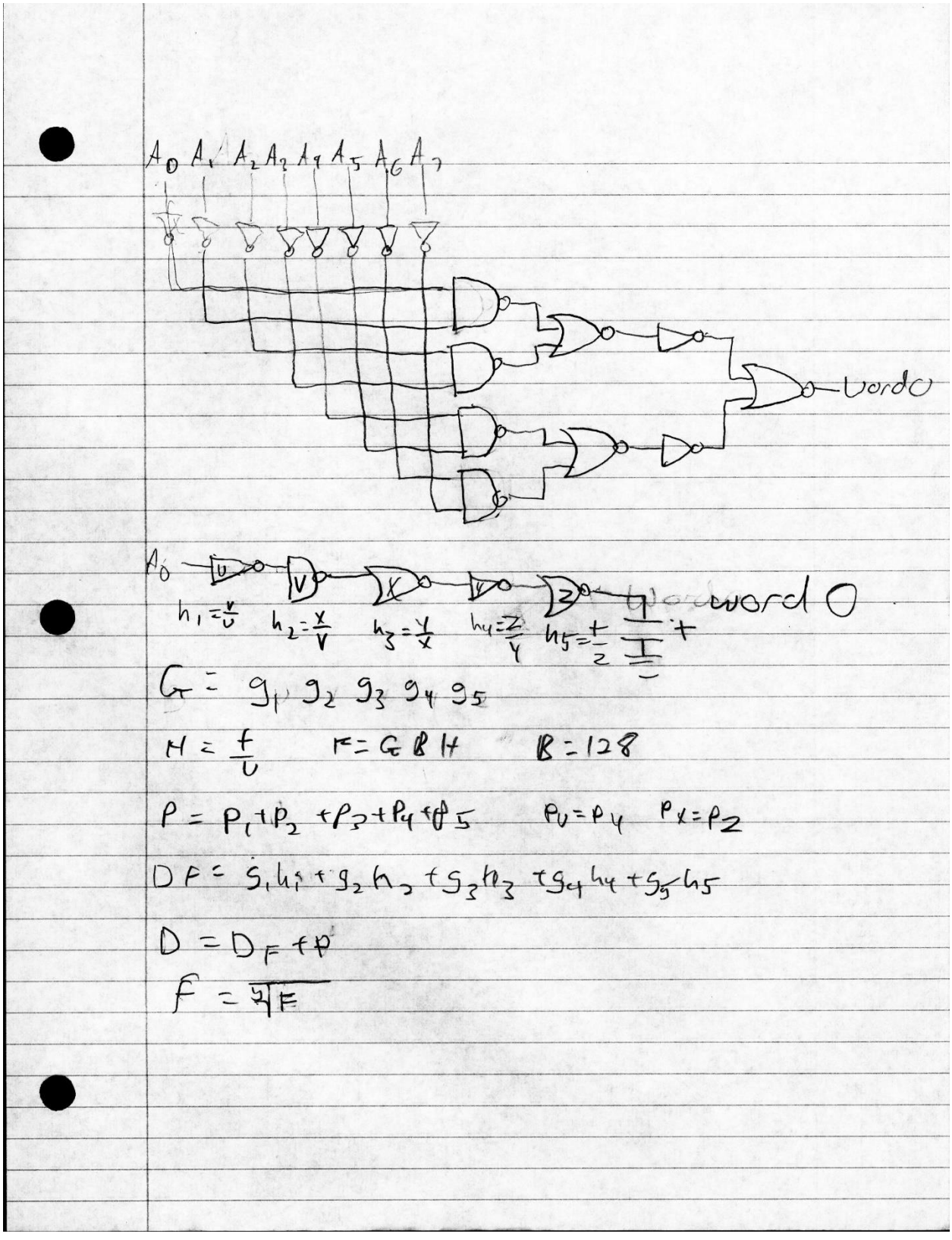
Gopal Hari
Brian Morris
Phillip Seaton

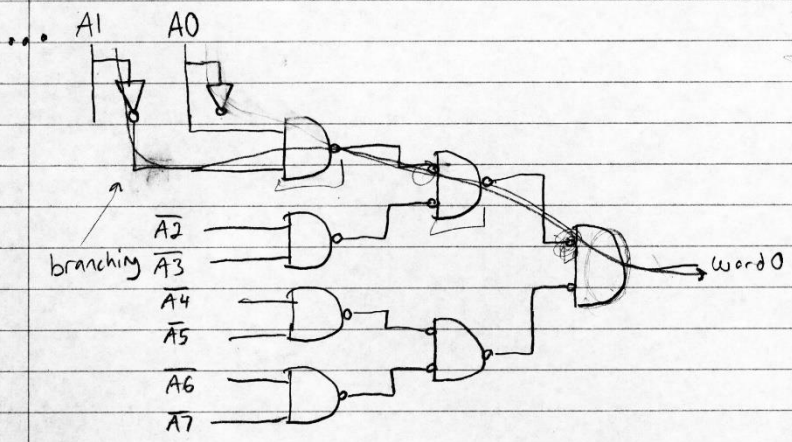
Decoder Analysis

Design 1:

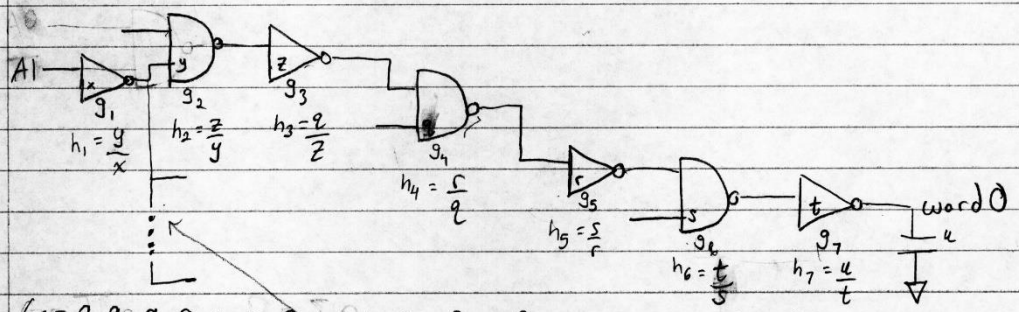


Design 2:

Using 2 input NANDs / Inverters



Critical Path using available gates:



$G = g_1 g_2 g_3 g_4 g_5 g_6 g_7$ $g_2 = g_4 = g_6$ $g_1 = g_3 = g_5 = g_7$

$H = \frac{u}{x_f}$

$F = GBH$ where $B = 128$ comes from inverter x

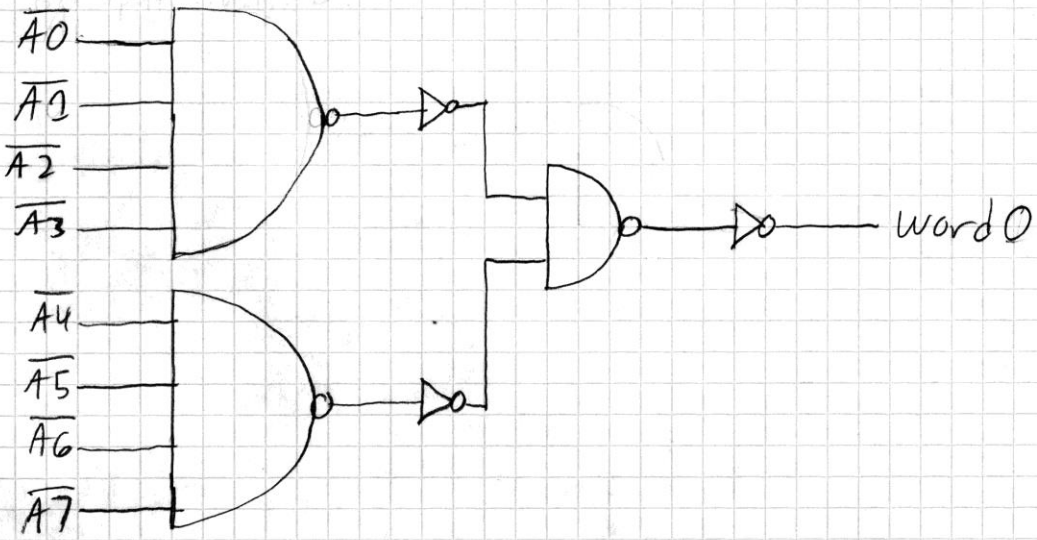
$P = P_1 + P_2 + P_3 + P_4 + P_5 + P_6 + P_7$ $P_2 = P_4 = P_6$ $P_1 = P_3 = P_5 = P_7$

$D_F = (g_1 h_1) + (g_2 h_2) + (g_3 h_3) + (g_4 h_4) + (g_5 h_5) + (g_6 h_6) + (g_7 h_7)$

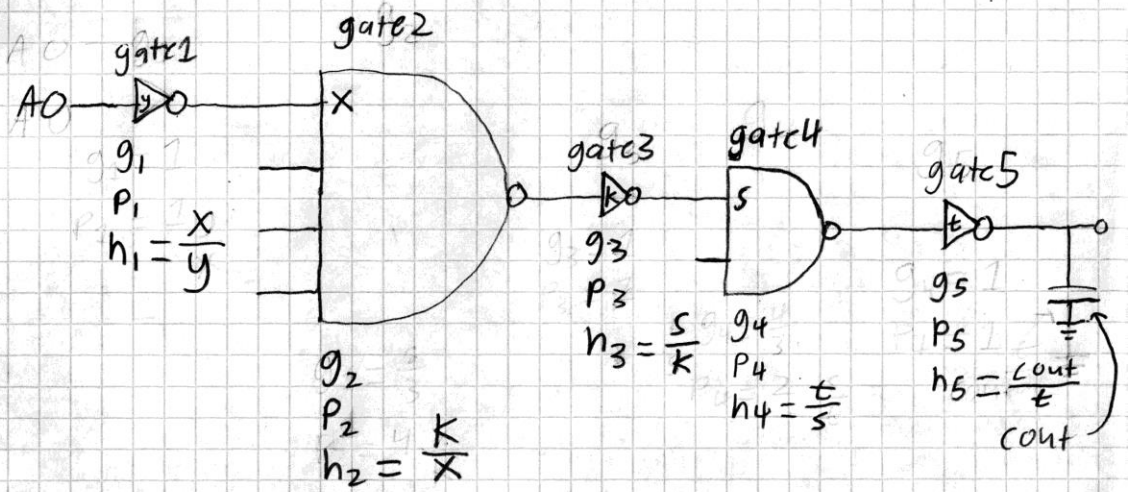
$D = D_F + P$ $\hat{f} = \sqrt[7]{F}$

Design 3:

Using 4-input NANDS, 2-input NANDS, and Inverters



Critical path:



$G = g_1 \cdot g_2 \cdot g_3 \cdot g_4 \cdot g_5$ $\quad H = \frac{cout}{y}$ $\quad B = 128$ (from gate1)

$P = P_1 + P_2 + P_3 + P_4 + P_5$ $\quad \hat{f} = \sqrt[5]{F}$

$D_F = (g_1 h_1) + (g_2 h_2) + (g_3 h_3) + (g_4 h_4) + (g_5 h_5)$ $\quad D = D_F + P$

Design 1 Calculations:

$G = g_2 g_3 g_4 g_5 = 1.465 * 0.83 * 1 * 0.83 = 1.009$

$P = p_2 + p_3 + p_4 + p_5 = 1.57 + 2.09 + 1 + 2.09 = 6.75$

$H = \frac{512}{3}$

$B = 64$

$F = GHB = 11020.97$

$f' = F^{\frac{1}{4}} = 10.25$

$D = Nf' + P = 47.73$

Design 2 Calculations:

$G = g_2 g_3 g_4 g_5 g_6 g_7 = 1.465 * 1 * 1.465 * 1 * 1.465 * 1 = 3.14$

$P = p_2 + p_3 + p_4 + p_5 + p_6 + p_7 = 1.57 + 1 + 1.57 + 1 + 1.57 + 1 = 7.71$

$H = \frac{512}{3}$

$B = 64$

$F = GHB = 34297.173$

$f' = F^{\frac{1}{6}} = 5.70$

$D = Nf' + P = 41.91$

Design 3 Calculations:

$G = g_2 g_3 g_4 g_5 = 2.155 * 1 * 1.465 * 1 = 3.157$

$P = p_2 + p_3 + p_4 + p_5 = 2.86 + 1 + 1.57 + 1 = 6.43$

$H = \frac{512}{3}$

$B = 16$

$F = GHB = 8621$

$f' = F^{\frac{1}{4}} = 9.6358$

$D = Nf' + P = 44.9732$

We are choosing design 3 for several reasons. First of all the g value for NOR seems incorrect (0.83) as it is less than that of an inverter. This caused our G value for Design 1 to be skewed. Looking at Design 2 and 3, which did not use NOR gates, we can see that Design 2 has a lower delay, however it utilizes 6 stages and many more gates. This will result in more area required for the layout which is undesired. This led us to choose design 3, which had a slightly larger delay but fewer stages, meaning a more compact layout.